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24. (New) The semiconductor device of claim 20, wherein a gap or clearance is defined between the first and second insulating layers adjacent an area where the conductive materials are solid-state-bonded to one another.

REMARKS

This is in response to the Office Action dated March 19, 2002. Claims 2 and 10-19 have been canceled. New claims 20-24 have been added. Thus, claims 1, 3-9 and 20-24 are now pending. Attached hereto is a marked-up version of the changes made to the claim(s) by the current amendment. The attached page(s) is captioned "**Version With Markings To Show Changes Made.**"

For purposes of example and without limitation, certain example embodiments of instant elected invention relate to a semiconductor device including first and second portions which are solid state bonded to each other. Referring to Figures 1-4 of the instant application, the first portion 100 includes a semiconductor substrate 1 which supports a wiring layer 3, insulating layer 7, and conductive regions 5, 6. Conductive region 5 is provided in a through-hole 13 defined in insulating layer 7, while conductive region 6 is in the form of a wiring layer provided on top of insulating layer 7. Because of chemical mechanical polishing (CMP) for example, the exposed surfaces of conductive regions 5, 6 are at least partially concave in shape so as to define dishing portions (e.g., see reference numeral 17 which indicates a dishing portion). In this first portion 100, etching (e.g., RIE) as shown in Figures 2a-2c is used in order to lower the exposed surface of through hole insulating portion(s) 11 relative to the exposed surface of

conductive regions 5, 6. As a result, at least part of the exposed concave surfaces of conductive regions 5, 6 protrude outwardly from the exposed surface of through hole insulator region 11. The second portion 200 is formed in a similar manner. Then, as shown in Figures 3-4, the first portion 100 and second portion 200 are pressed together using force F in order to solid state bond the concave shaped dishing portion(s) of conductive regions 5, 6 of the first portion 100 to the conductive regions 25, 26 of the second portion 200. A clearance (or gap) 30 may be left between the first portion 100 and second portion 200 in areas adjacent the respective through-hole insulator regions 11, 21 where no conductive region is provided, in certain instances. Accordingly, the conductive regions are securely and/or directly bonded to each other even though the dishing portions exist in these conductive regions. A high reliability electrical connection of the conductive regions can be realized (see page 7, lines 5-13; and page 13, lines 18-21).

Claim 1 stands rejected under 35 U.S.C. Section 102(b) as being allegedly anticipated by Kawai (US 5,939,789). This Section 102(b) rejection is respectfully traversed for at least the following reasons.

Claim 1 requires "a first portion comprising a first substrate, a conductive layer and an insulating layer laminated on the first substrate and a bonding surface that is chemically mechanically polished and exposes a conductive region and an insulating region, wherein the *conductive region includes a concave surface defining a dishing portion*; a second portion comprising a second substrate, a conductive layer and an insulating layer laminated on the second substrate and a bonding surface that is

chemically mechanically polished and exposes at least a *conductive region having a concave surface defining a dishing portion*; and wherein the bonding surface of the first portion and the bonding surface of the second portion are *solid-state-bonded to each other so that the dishing portions of the conductive regions of the respective first and second portions are bonded to each other so as to contact one another* . . . ." For example, see Fig. 3 of the instant application which illustrates opposing concave dishing portions 17 which are to be solid state bonded to one another. Kawai fails to disclose or suggest the aforesaid underlined aspects of claim 1.

Kawai in Fig. 12(c) illustrates Cu filled through holes 4 provided in insulating films 1, which are in electrical communication with one another via metal wirings 2 and Sn bonding members 5. However, Kawai significantly differs from the invention of claim 1 in that the Cu material which fills through holes 4 in Kawai *does not have a dishing portion (i.e., it has no concave shaped surface).* Thus, respective dishing portions (i.e., having concave surfaces) cannot possibly be directly bonded to one another in Kawai. Since Kawai has no concave dishing portions, claim 1 cannot be anticipated or otherwise rendered unpatentable over Kawai. Kawai is entirely unrelated to the invention of claim 1 in this regard.

New claim 20 states that "the first conductive material that fills in the contact hole in the first insulating layer and the second conductive material that fills in the contact hole in the second insulating layer are solid-state-bonded to each other so as to *contact* one another in a bonded state." For example, Figs. 3-4 of the instant application illustrate that the conductive material 5 in contact hole 13 of insulating layer 7 is solid-state-

bonded to and *contacts* the conductive material 25 provided in through hole 28 of the other insulating layer 27. Kawai fails to disclose or suggest this aspect of claim 20. In particular, Kawai's requirement of tin bonding members 5 and metal wirings 2 means that in Kawai the material which fills opposed through holes 4 in Kawai is *not* directly bonded to each other and thus is in *non*-contacting relation. Kawai thereby teaches directly away from, and is unrelated to the invention of claim 20.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are believed to be in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please cancel non-elected claims 2 and 10-19, without prejudice in view of the Restriction Requirement.

1. (Amended) A semiconductor device comprising:

a first portion [having] comprising a first substrate, a conductive layer and an insulating layer laminated on the first substrate and a bonding surface that is chemically mechanically polished and exposes a conductive region and an insulating region, wherein the conductive region includes a concave surface defining a dishing portion;

a second portion [having] comprising a second substrate, a conductive layer and an insulating layer laminated on the second substrate and a bonding surface that is chemically mechanically polished and exposes at least a conductive region having a concave surface defining a dishing portion; and wherein

the bonding surface of the first portion and the bonding surface of the second portion are solid-state-bonded to each other so that the dishing portions of the conductive regions of the respective first and second portions are bonded to each other so as to contact one another, and

at least one of the bonding surface of the first portion and the bonding surface of the second portion has the insulating region lowered with respect to the conductive region.

Please add the following new claims:

20. (New) A semiconductor device comprising:

a first substrate supporting a first insulating layer with a contact hole defined therein, and a first conductive material filling in the contact hole in the first insulating layer and protruding above a surface of the first insulating layer;

a second substrate supporting a second insulating layer with a contact hole defined therein, and a second conductive material filling in the contact hole in the second insulating layer; and

wherein the first conductive material that fills in the contact hole in the first insulating layer and the second conductive material that fills in the contact hole in the second insulating layer are solid-state-bonded to each other so as to contact one another in a bonded state.

21. (New) The semiconductor device of claim 20, wherein the second conductive material filling in the contact hole in the second insulating layer protrudes above a surface of the second insulating layer.

22. (New) The semiconductor device of claim 20, wherein the first and second conductive materials are of the same material.

23. (New) The semiconductor device of claim 20, wherein concave surfaces of the respective first and second conductive materials are bonded to one another so as to contact each other.

24. (New) The semiconductor device of claim 20, wherein a gap or clearance is defined between the first and second insulating layers adjacent an area where the conductive materials are solid-state-bonded to one another.